**Midterm Exam**

Note : Please Follow the solution template in answering the exam, No answers will be accepted without the solution template.

## Q1. Floor planning practical Tutorial:

In this stage we will perform floor planning on the design, you suppose to finish setup stage before starting floor planning stage and [counter.dlib] should be present in your directory.

1. Go to the pnr folder in your project directory and open IC Compiler || and GUI.
2. From the GUI choose -> open block then :

Library name -> counter.dlib [design library generated in the setup stage]

Block name -> select pit\_top then ok

Now you will find the block opened with the standard cells from the design.

1. Write the following command in the icc2\_shell

set\_parasitic\_parameters -late\_spec maxTLU -early\_spec minTLU

1. **Initialize floor plan**

From Task menu choose Design planning then floor plan initialization

Leave all the default options :

Boundary -> core area

Type ->Rectangle

Side size control -> Ratio

Aspect ratio -> 1

Then in [space between core and die areas ] Uniform part put 10

Sides a =1 , b=1

Core utilization -> 0.6

Then press apply.

Now the core is created with utilization =60 %

Unplacing all cells

Creating site arrays

Creating routing tracks

Initializing floorplan completed.

1. **Create Placement**

From Task menu -> Design Planning -> Cell Placement -> Cell Placement

Check [ use floor planning placement]

Then Apply

You will find the standard cells placed inside the blocks.

1. **Pins Constrains**

* We need to specify certain metal layers allowed for pin placement.

From Task menu -> Design Planning -> Pin Assignment -> Block Pin Constrains ->

Create\_clock\_pin\_constrains

In allowed layers -> choose M3, M4, M5, M6

* We need to place the pins

From Task menu -> Design Planning -> Pin Assignment -> Place Pin/Global Route /Congestion

Check [Place only top level ports]

Then Apply

You will find the ports placed around the edges of the die.

1. Finally saving the block , write the following command in the shell

save\_block counter.dlib:pit\_top.design

1. Collect all the commands written in the console in a script called floorplan.tcl

## Q2) Task 1

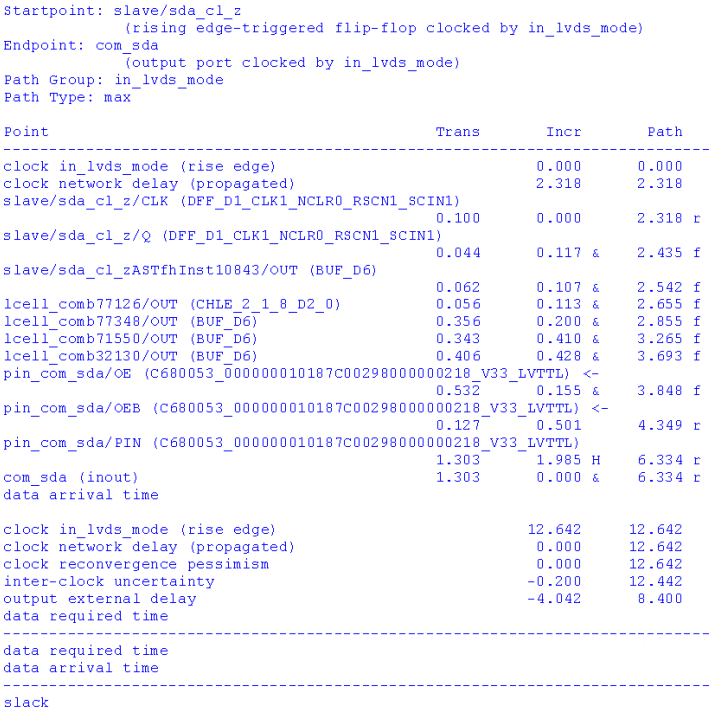
In the following timing report:

1-what is the type of timing path?

2-calculate the propagation?

3- calculate Tc2q, slack?

4- what is the max frequency?



## Q2) Task 2

In the following timing report:

1-what is the type of timing path?

2- Calculate the slack, obtain any violations?

